

AD-R100 761

TECHNOLOGY DEVELOPMENT OF A PLANAR BIPOLAR TRANSISTOR  
(U) THOMSON COMPONENTS-MOSTEK CORP MONTGOMERYVILLE PA  
P MIGUELEZ 1987 N00014-86-C-2523

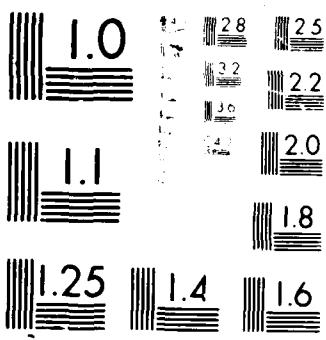
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AD-A188 761

PROGRESS REPORT

TECHNOLOGY DEVELOPMENT OF A  
PLANAR BIPOLAR TRANSISTOR

CONTRACT # N00014-86-C-2523

Reporting Period: 1 October 1986 to 1 December 1986

CDRL ITEM A001

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DEC 30 1987  
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THOMSON COMPONENTS - MOSTEK CORPORATION  
Commerce Drive  
Montgomeryville, PA 18936

DISSEMINATION STATEMENT

Approved for public release  
Distribution Unlimited

## PROGRESS REPORT

1. Contract - N00014-86-C-2523
2. Project Title - Technology Development of a Planar BiPolar Transistor
3. Project Objective - Develop and demonstrate a Silicon Planar BiPolar Transistor incorporating isolation techniques to achieve an improvement in thermal resistance which supports designs for longer pulse widths and duty factors.
4. Period Covered - 1 October 1986 to 1 December 1986
5. Location of Work - Thomson Components - Mostek Corporation Montgomeryville, PA
6. Responsible Individual - Phil Miguelez  
Thomson Components - Mostek Corporation  
Commerce Drive  
Montgomeryville, PA 18936  
(215) 362-8500
7. Milestone Chart - Updated to show work accomplished.
8. Work Accomplished

### TASK 1 - TRANSISTOR DESIGN

A new transistor die geometry was designed incorporating top collector contacts and intrinsic backside isolation. Unique features of this design include:

- \* High emitter periphery to base area Figure of merit (10) vs typical L-Band geometries (4.5 - 6.5).
- \* "End - Fed" top collector contacts to reduce collector contact resistance.
- \* Individual common lead contacts to reduce common lead inductance.
- \* Emitter site ballasting as well as collector ballasting to minimize cell to cell temperature variations.
- \* Tri-layer structure consisting of an insulator sub-layer, epitaxial buried layer, and epitaxial collector top layer.



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Figure 1 depicts the conceptual geometry lay-out, while Figure 2 shows details of the cell structure including proposed concentration levels. Drawings have been delivered to the mask vendor and digitizing for mask set generation is underway.

### **TASK 3 - PACKAGE DESIGN**

A visit was made to the package vendor on November 20, 1986 to discuss design aspects of the proposed transistor package. It has been decided to delay final tooling of the package until preliminary RF test results can be obtained and internal metallization patterns to optimize RF performance can be defined. Package piece parts have been ordered conforming to the proposed package concept. These piece parts consisting of lead frame, alumina window frame, heat spreaders, and flanges will be assembled by TCMC in order to evaluate relative design advantages and further define the final package design.

#### **9. Plans -**

Upon verification of the delivered mask set, two wafer lot starts will be initiated consisting of a top collector lot and a non-top collector (control) lot used to verify the geometry/process design.

**FIGURE 1**  
**PROPOSED ISOLATED TOP COLLECTOR GEOMETRY**

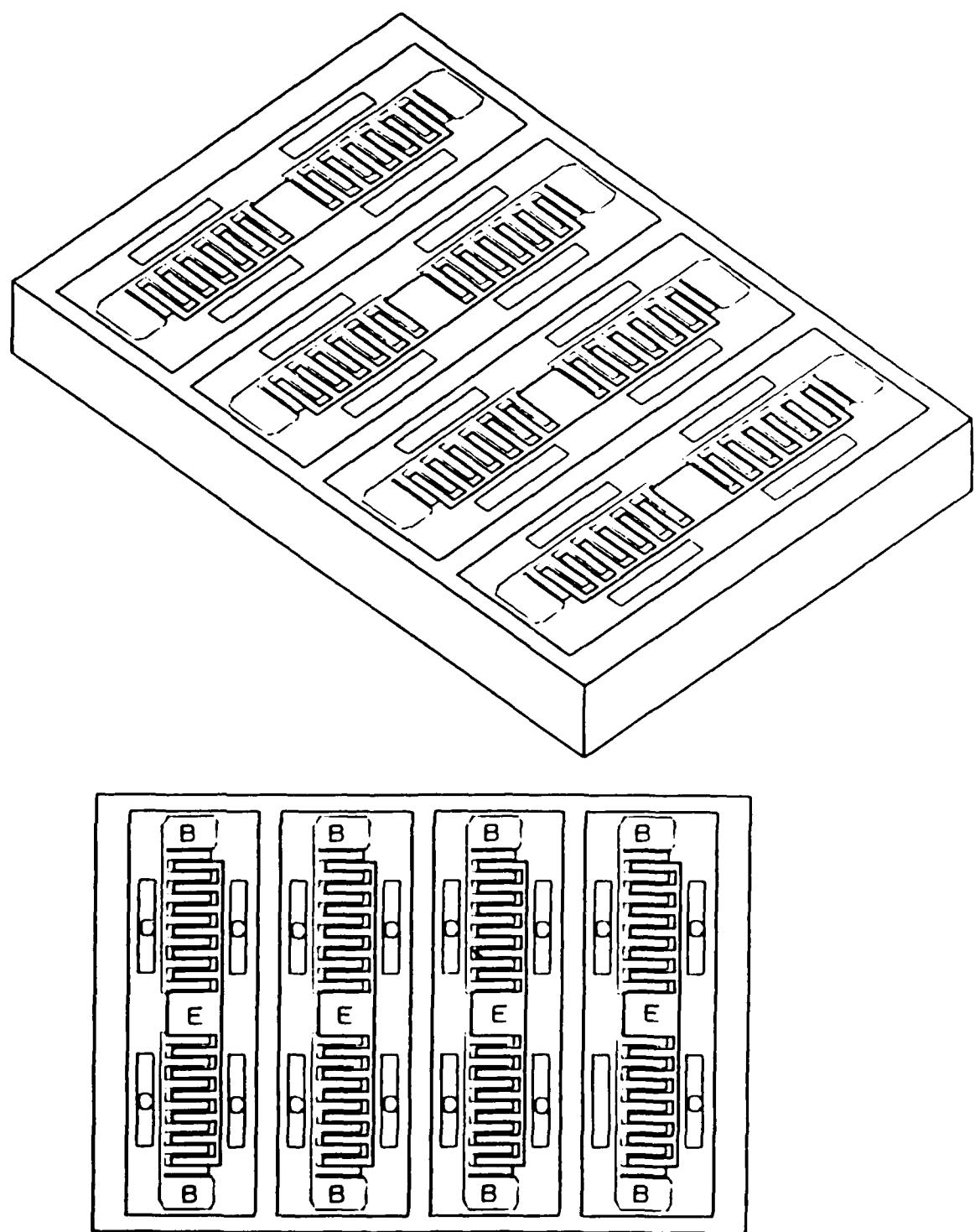
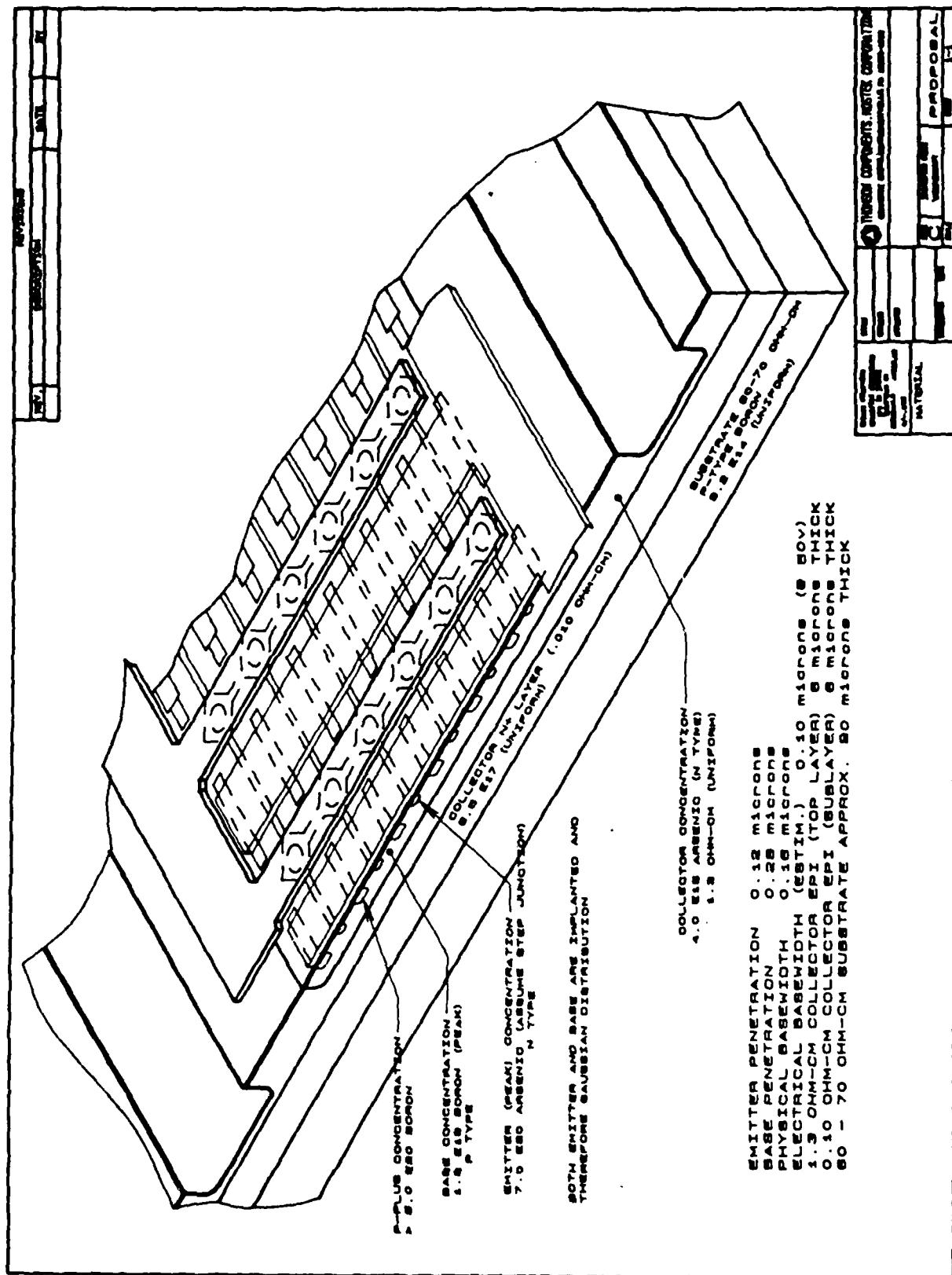


Figure #2



**Figure 3**

ENGINEERING PROJECT Isolated Collector Planar Bipolar Transistor

September 25, 1986	Months A.R.O.
Description	
1. Mask Set Design of Top Collector Die	
2. Package Redesign (Piece Part Assembly)	
3. Package Deliveries (Lead Assemblies, Diamond Heat Spreaders)	
4. Wafer Material Deliveries (1-1-1) and (1-0-0)	
5. Trial Runs of (1-1-1) and (1-0-0) Non-Top Collector Wafer Lots (for targeting only)	
6. Electrical Evaluations	
7. 1st Group Runs of Top Collector, Isolated Material Wafer Lots	

**CONTRACT EXPENDITURES**

1.	Contract Award	-	\$433,280.00
2.	Funds Released	-	\$155,000.00
3.	Cost Summary:		
	Billing No.	1	
	Month	11/86	
	Total Monthly Billing		\$33,927.00
	Total Cumulative Billing		\$33,927.00
	% of Released Funds		21.89

END  
DATE

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MARCH  
1988

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